WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array in which memory cells each having six transistors are arranged two-dimensionally on a semiconductor substrate;

a plurality of word lines connected to each of the memory cells, and arranged on a parallel to each other along a first direction;

a plurality of bit lines connected to each of the memory cells and arranged on a parallel to each other along a second direction perpendicular to the first direction; and

at least two gate electrodes provided on the semiconductor substrate such that each of the gate electrodes is connected to at least one transistor of the six transistors, all of the gate electrodes being arranged on the same straight line parallel to the first direction.

2. A semiconductor memory device according to claim 1, wherein all gate electrodes in two memory cells adjacent to each other in the first direction are arranged on the substantially same straight line.

3. A semiconductor memory device according to claim 1, wherein each of the gate electrodes has a rectangular configuration having sides of straight line.

4. A semiconductor memory device according to claim 1, wherein the semiconductor memory device has a laminated structure in which layers are laminated on the semiconductor substrate and a ground surface serving as a ground of each memory cell is formed on the uppermost surface of the laminated structure.

5. A semiconductor memory device according to claim 1, wherein the six transistors comprises first and second sets of driver transistor, load transistor

and access transistor, and the gate electrodes comprises:

a first gate electrode connecting the driver transistor and the load transistor of the first set;

a second gate electrode connecting the driver transistor and load transistor of the second set;

a third gate electrode connected to the access transistor of the first set; and

a fourth gate electrode connected to the access transistor of the second set,

wherein the third electrode, the first electrode, the second electrode, and the fourth electrode are respectively arranged from the one end of the straight line to the other end of the straight line.

6. A semiconductor memory device according to claim 5, further comprising:

a first connector connecting first gate electrode to an active region of the driver transistor of the second set and an active region of the load transistor of the second set;

a second connector connecting first gate electrode to active region of the driver transistor of the first set and an active region of the load transistor of the first set;

a third connector connecting the third gate electrode and the word line; and

a fourth connector connecting the fourth gate electrode and the word line,

wherein the first and second connectors respectively include parts which

are parallel to the all of the gate electrodes.